Crystal DSP Board Operation and Test Debug

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1 Introduction

The Crystal DSP board (hereafter referred to as the DSP board) replaces the Motorola DSP board in the Citation 5.0 as the digital decoder. It is used in the Signature 2.0 and Festival 100 also. The DSP board currently supports:

- Dolby Digital (supported only as compressed digital inputs)
  - “Coaxial” (or good quality audio cable) SPDIF inputs from four phono jacks.
  - TOSLINK (optical) SPDIF inputs from two TOSLINK receiver inputs.
- DTS (supported only as compressed digital inputs)
  - “Coaxial” (or good quality audio cable) SPDIF inputs from four phono jacks.
  - TOSLINK (optical) SPDIF inputs from two TOSLINK receiver inputs.
- Pro Logic (supported by digital PCM inputs or analog inputs)
  - “Coaxial” (or good quality audio cable) SPDIF inputs from four phono jacks.
  - TOSLINK (optical) PCM inputs from two TOSLINK receiver inputs.
- Stereo and Monaural (supported by digital PCM inputs or analog inputs)
  - “Coaxial” (or good quality audio cable) PCM inputs from four phono jacks.
  - TOSLINK (optical) PCM inputs from two TOSLINK receiver inputs.
- Special effects modes (i.e., MOVIE 1-4 and MUSIC 1-4)

Citation 5.0 does not provide analog inputs to the DSP BOARD. Signature 2.0 and Festival 100 products support analog inputs to the DSP board.

Future support of new modes is possible (e.g., Logic 7) with a Crystal DSP board PROM and 80C251 CPU PROM. THX support is possible with a PROM upgrade and the addition of a plug-on expansion DSP board module. The expansion DSP board module support is designed into the current DSP board design.

2 DSP BOARD Operation

Each DSP board design schematic page represents a major board function. Each schematic page function is described in this section.

2.1 Power

- The Ferrite bead, FB1, attenuates any +5V digital switching noise that might go back to the power supply and affect analog voltages.
- The MIC2937A regulator generates +3.3V from the +5V supply for the 3.3V Crystal DSP chip.
- The larger tantalum capacitors help “hold” up the power supply voltages for sudden large changes in current demand on the DSP board.
- The paralleled smaller mica capacitors bypass higher frequency power supply noise.
- The “GND VIA” is the schematic representation of the large via that the mounting bracket is attached to. This via is connected directly to the digital ground plane. This provides a connection between the chassis and the digital ground to help contain the 50 MHz digital switching EMI emissions inside the box.
- Power and ground on the board is distributed on internal PCB planes.
  - Layer 2 is the Ground plane (the layer right under the top component side layer). The ground plane is split into two sections; the digital ground plane and the analog ground plane.
    - The digital ground plane section provides a ground reference to all digital parts. It takes up all the space under the digital logic
    - The analog ground plane section provides a ground reference to all analog (Op Amp-related) parts. It takes up all the space under the analog section (Op-Amps and components).
    - The digital and analog planes are separated by a 1/8” gap to isolate the digital switching noise from the analog section.
    - The two planes are tied together at one point with a copper “bridge” about ½” wide. This provides a return path for common signals between the digital and analog domains.
  - Layer 3 is the Power plane (the layer between the Ground Plane and the Layer 4 solder side). The power plane is split into five sections:
    - +5VD –- most of the board digital logic is driven off this plane section. It takes up all the room under the digital logic except for the +3.3V plane “island”.
    - +3.3VD –- this is an isolated “island” surrounded by the +5V plane section. The 3.3V planar section provides power to the Crystal DSP chip and supporting +5V/3.3V buffers to interface with the +5V logic on the board.
    - +5VA –- this planar section provides +5V to the CODEC. It is sourced from the +5VD section above, but is isolated by the FB8 ferrite bead.
    - +15VA – this planar section provides power to the analog Op Amps. It takes up half of the space available under the analog section.

- -15VA – this planar section provides power to the analog Op Amps. It takes up half of the space available under the analog section.
- The digital and analog planes are separated by a 1/8″ gap to isolate the digital switching noise from the analog section.
- NONE of the power planes are tied directly together, unlike the ground planes.

2.2 Clock/Reset

This function provides the digital clocks for the board and provides the power-up Reset signal for the digital logic.

2.2.1 Clock Generator

The Crystal DSP chip requires a 50 MHz clock. This is generated by a 50 MHz oscillator component. It is divided down by 4 to get the 12.288 MHz clock used by the CODEC and the 80C251 Micro Controller. The 50 MHz clock is series terminated at the oscillator output. No capacitor is used to slow down the edges (which would reduce EMI emissions) because it fouls up the 50 MHz clock duty cycle going through the clock buffers. The clock duty cycle is critical for the DSP chip and must be no worse than 60/40%. We have even had to specify a particular clock buffer chip (Toshiba). The equivalent Motorola buffer skewed the duty cycle too much and the DSP chip doesn't operate reliably in all cases (one board out of twenty prototypes failed with the Moto part).

2.2.2 Reset Generator (Power Monitor)

The TL7705A is a power monitor chip that generates a Reset pulse of specified minimum width when power is initially brought up or "glitched". The TL7705A also asserts DSP board RESET continuously while the external RESET signal is asserted. This happens when the System CPU (i.e., Citation, Signature, or Festival CPU) asserts the Reset signal that is brought over on the "serial communication" cable connector (EXTRESET on connector P1).

- It should be noted that if System (i.e., Citation, Signature, or Festival) power is "glitched" and the System CPU does not get Reset the system could "hang". The DSP board would be Reset and waiting for setup commands from the System CPU, while the System CPU (IF not Reset also) would think it had already set up the DSP board.
- From a user's point of view, if a power "glitch" occurred during playback of an AC-3 (Dolby Digital) source the System (Citation, etc) could go silent in this case.

2.3 SPDIF Input

The SPDIF input function conditions phono jack SPDIF signal inputs and selects one of 4 phono inputs or one of 2 TOSLINK inputs for the single CODEC SPDIF input.

- The phono jack SPDIF inputs have EMI filtering (FL1, R12, C19 is typical) to provide 75 ohm termination and to suppress conducted EMI out the connected input cable. Each input is capacitively coupled (C18 is typical) to a CMOS multiplexer. One of four typical phono

jack 400 mV SPDIF input signals is selected by the DSP board CPU using the 3 control bits (6 total SPDIF inputs). The selected signal is passed directly to the CODEC SPDIF input.

- The TOSLINK SPDIF inputs have only a 100 Ohm isolation resistor to the CMOS input. One of two typical TOSLINK 5.0V SPDIF input signals is selected by the DSP board CPU using the 3 control bits. The selected signal is passed directly to the CODEC SPDIF input. The CODEC is capable of processing a signal within the range of 400 mV to 5V.

2.4 CPU

The DSP board requires a control microprocessor to:

- Communicate with the System CPU for operating mode, input selection, and error reporting.
- Setup and monitor operation of the DSP board chip and CODEC chip.

The CPU function consists of the Micro Controller chip, external program memory EPROM, and DSP board I/O signals.

2.4.1 Micro Controller Chip

The DSP board uses an Intel 8xC251 family micro controller. It was designed to support either the 87C251 with no external PROM or the 80C251 with external PROM. It turns out that the 80C251 and an external PROM is cheaper than the 87C251 alone so the current released board has been modified to support only the 80C251 with external program memory PROM (a connection has been made between R85 and C56 closest to the 80C251 socket to force external PROM access).

- NOTE: The Micro Controller Configuration Bytes must be setup as follows:
  - Config Byte 0 – 0xDB
  - Config Byte 1 – 0xF6
- These bytes are setup in external memory location 0xFFF8 and 0xFFF9, respectively. The Micro Controller will fetch these values upon encountering a hard RESET.
- The function of these bytes is described in Intel’s literature, but it specifies such factors as wait states or not for external memory and other hardware dependent configuration.

2.4.2 Micro Controller External PROM

The U32 PROM contains the Micro Controller program code. It is supported with an address latch and PROM device.

- Address Latch – Micro Controller uses the ALE signal to indicate when a valid external memory address is on the Multiplexed ADDR/DATA bus. This signal clocks the address into an address latch for addressing the PROM
- PROM – a variety of PROM sizes and types can be used for this location.
  - One Time Program PROM or FLASH PROM types supported
  - 256K or 512KB sizes are supported (only the low 64KB is used). Smaller PROM sizes are not form factor compatible and the design

intent was to be able to use the same PROM for both the CPU and DSP Proms if desired.
- For Production, the AM27C010 256KB OTP PROM is used for cost.

2.4.3 Micro Controller I/O

The 80C251 drives a number of input or output control signals via its' I/O ports Port 1 and Port 3. These signals include types of:

- SPI interface (serial peripheral interface supporting communication between the CPU and the DSP and CODEC).
  - SPISCLK –- SPI bus clock
  - MOSI –- SPI serial data out of the CPU to peripheral chips.
  - MOSI –- SPI serial data into the CPU from peripheral chips.
  - \DSPCS –- DSP SPI chip select.
  - \CDCS –- CODEC SPI chip select.
  - \EXPCS –- Expansion DSP (on external plug-on board) SPI chip select.
- Peripheral Chip Software controlled Reset
  - DSPCPURESET –- DSP chip Reset.
  - CDCPURESET –- CODEC chip Reset.
  - EXPCPURESET –- Expansion DSP chip Reset.
- "RS-232" format I/O port for System CPU communication
  - RXD
  - TXD
  - Note that the System CPU RESET signal for the DSP board is brought in on Pin 1 of the P1 "RS-232" connector. This signal allows the System CPU to hold the entire DSP board in Reset (DSP board outputs are muted).
- Interrupt Inputs
  - \DSPIRQ –- DSP chip interrupt. The DSP chip interrupts the CPU to notify it of completion of auto-booting or a change in status in the audio digital signal bit stream.
  - \EXPIRQ –- Expansion DSP chip interrupt. The DSP chip interrupts the CPU to notify it of completion of auto-booting or a change in status in the audio digital signal bit stream.
  - There is no interrupt input from the CODEC.
- DSP Auto Boot Control
  - ABOOT –- one of the signals used to direct auto booting of the DSP. Details are described in the CPU 'C' code firmware comments.
- Micro Controller PIO Expansion I/O Port "A" Control
  - This is an external chip added to increase the number of I/O Port bits available for the Micro Controller. There weren't enough I/O port bits available within the Micro Controller itself.
  - EXP_PIOA_PARALLEL_LOAD –- controls loading information into the external serial to parallel chip under control of the Micro Controller firmware.
  - Note that the SPISCLK and MOSI SPI bus signals are also used to communicate with the expansion I/O port chip as well as the DSP chip and CODEC chip.
- Micro Controller PIO Port "A" Control Signals
  - Signals are driven by Micro Controller code.

- SPMUXCTL0-2 –- The three SPDIF MUX address control bits. These bits select which of 6 SPDIF inputs are routed to the CODEC.
- \DSPMUXSEL –- This bit selects which DSP I2S outputs are routed to the CODEC. This is necessary to accommodate support of an expansion DSP for something like THX post processing.
  - \DSPMUXSEL = 0 selects the MAIN DSP outputs to the CODEC. This configuration is used for all applications except those which require post-processing, like THX.
  - \DSPMUXSEL = 1 selects the EXPANSION DSP outputs to the CODEC.
    - For THX, the MAIN DSP will complete most signal processing, pass the processed signal on (via its' I2S output) to the Expansion DSP, which will do the THX post processing and then the Expansion DSP outputs will be sent to the CODEC.
- \uC15-18 –- These four bits select the DSP PROM Page address to point to one of sixteen 32KB pages for different DSP code algorithms (or DSP tables like DTS tables). Each DSP code algorithm set consists of a maximum of 32KB of code.
  - The exception to this is that DTS tables require 64KB. How this is handled is described in the section on the DSP "EPROM" function.
- EXP_PIOA_SERDATOUT –- This signal is used currently only for the Festival 100 product.
  - It allows the DSP board CPU to control another parallel I/O port on one of the Festival boards for digital tone control.
  - NOTE that the 6-pin JP4 connector is used exclusively for this interface on Festival. There is no other use for JP4.

2.5 DSP/CODEC

This function consists of the DSP and CODEC chips and some 5V to 3V buffers for interfacing the 3.3V DSP chip to the +5V CPU chip.

2.5.1 DSP Chip

The Crystal DSP chip is the heart of the DSP board digital decoder function. The DSP chip supports the following functions:

- Auto boot –- the DSP chip executes its' microcode from an internal 32KB RAM. This RAM is downloaded from an external EPROM. The DSP chip will automatically read in the currently selected 32KB page of external memory when the CPU initiates the DSP auto boot sequence. This auto boot of code takes about 80 msec, plus some other setup delays. So, it takes about 100-200 msec to auto boot or switch modes. The user sees this minor delay when switching from one mode type to another via the User Interface (remote control of On Screen Menu).
  - \EXTMEM – External memory access enable
  - \EMOE – External memory data output enable
  - D0-D7 – Multiplexed external memory address / data bus.
- Sharing Auto Boot EPROM –- two DSPs (MAIN and EXPANSION) share the same boot PROM when both are present. This keeps the expansion DSP board very simple and inexpensive.
- SPI bus communication interface –- the DSP communicates with the CPU via a SPI protocol. This simple serial interface requires only a

data line, clock, and chip select. The communication protocol is hard-wired into the DSP chip (it works before the DSP is auto booted) and in the CPU is handled in firmware.

- SCCLK –- SPI Clock input
- SCDIN –- SPI data input
- SCDOUT –- SPI data output
- SPI_CS –- SPI chip select
- \INTREQ – Although not SPI-related, this interrupt in a CPU communication signal.

- Input Audio Data Bit stream
  - IEC937 serial data inputs
    - SDATAN1 and SDATAN2 – These inputs are tied together in this application, although only one can be actively used at a time. It depends on the input mode as to which one is selected under CPU firmware control.
    - These inputs accept audio input IEC937 compressed (AC-3) or linear PCM (stereo or DTS) serial data streams from the CODEC, which the CODEC has extracted from the SPDIF input bit stream.
  - IEC937 Serial Clock
    - MCLK input is generated by the CODEC to clock the IEC937 data stream bits into the DSP chip for decoding.
- DAC data outputs from decoded input stream
  - AUDATA0 – Left, Right Front Channel I2S data to CODEC DACs.
  - AUDATA1 – LEFT, Right Surround Channel I2S data to CODEC DACs.
  - AUDATA2 – Center, Sub-Woofer Channel I2S data to CODEC DACs.
  - Note that these three signal lines are what is multiplexed by U16 to select either the MAIN DSP outputs to the CODEC DACs or the Expansion DSP outputs to the CODEC DACs.
  - I2S Serial Clock
    - The DSP generates the SCLK and LRCLK to clock the decoded I2S audio data outputs to the CODEC DACs.
      - SCLK output is the I2S bit clock rate (typically 384KHz).
      - LRCLK output is the I2S Left/Right frame clock rate (typically 48KHz).

2.5.2 DSP Chip 5V / 3.3V buffer Chips

The U18 and U35 chips are 3.3V buffer chips that have 5V tolerant inputs, unlike the DSP chip. These chips are used to buffer both ways (Input and Output) when connecting a DSP chip pin to a 5V part. These non-inverting chips perform no function except this voltage isolation function.

2.5.3 Expansion DSP Connector

The JP3 connector serves as the physical interface to an Expansion DSP module when it is needed later for THX or other post-processing. All signals necessary to interface the two DSP chips and for the expansion chip to provide outputs to the CODEC are provided as pins on this connector. The connector also provides clock and voltage for the DSP Expansion module.

2.5.4 CODEC Chip

The Crystal CODEC chip is the digital / analog focus of the DSP board digital decoder function. It incorporates a SPDIF receiver for the DSP data input, as well as supporting DAC and ADC functions. The CODEC chip supports the following functions:

- SPDIF Receiver for DSP
  - IEC937 serial data inputs
    - SDOUT1 – Depending on CODEC setup, this output provides either Compressed or Linear PCM serial data streams to the DSP as an audio input data bit stream.
    - SDOUT2 – Not used any longer in this application.
    - This input accepts audio input IEC937 compressed (AC-3) or linear PCM (stereo or DTS) serial data streams from the CODEC, which the CODEC has extracted from the SPDIF input bit stream.
  - IEC937 Serial Clock
    - CLKOUT output is extracted from the incoming SPDIF data stream by the CODEC to clock the IEC937 data stream bits into the DSP chip for decoding.
- DAC data inputs from DSP.
  - SDIN1 –- Left, Right Front Channel I2S data to CODEC DACs.
  - SDIN2 –- LEFT, Right Surround Channel I2S data to CODEC DACs.
  - SDIN3 –- Center, Sub-Woofer Channel I2S data to CODEC DACs.
  - I2S Serial Clock
    - The DSP generates the SCLK and LRCLK to clock the decoded I2S audio data outputs to the CODEC DACs.
      - SCLK output is the I2S bit clock rate (typically 384KHz).
      - LRCLK output is the I2S Left/Right frame clock rate (typically 48KHz).
- SPI bus communication interface -– the DSP communicates with the CPU via a SPI protocol. This simple serial interface requires only a data line, clock, and chip select. The communication protocol is hard-wired into the DSP chip (it works before the DSP is auto booted) and in the CPU is handled in firmware.
  - CDIN –- SPI data input
  - \CS –- SPI chip select
  - CDOUT –- SPI data output
  - CCLK –- SPI clock input
- DAC analog outputs
  - AOUT1 –- Left Front Channel DAC output
  - AOUT2 –- Right Front Channel DAC output
  - AOUT1 –- Left Surround Channel DAC output
  - AOUT1 –- Right Surround Channel DAC output
  - AOUT1 –- Center Channel DAC output
  - AOUT1 –- Subwoofer Channel DAC output
- ADC analog inputs
  - Used to digitize analog signal inputs for DSP processing (e.g., Pro Logic analog input). The CODEC sends the digitized signal as a Linear PCM stream to the DSP via the CODEC IEC937 output.
  - AINR+ -- Right Channel + Differential buffer input
  - AINR- -- Right Channel - Differential buffer input
  - AINL- -- Left Channel - Differential buffer input

- AINL+ -- Left Channel + Differential buffer input

2.6 EPROM MEMORY

This memory is the DSP external program memory. Included are the EPROM, address latches, and an output data buffer.

2.6.1 EPROM memory

- An AMD 27C020 is used for the DSP micro code boot memory. The AM27C020 provides 512KB organized as follows:
  - 8 – 32KB pages for DSP microcode storage
  - 4 – 64KB pages for external DSP tables, such as DTS tables.
    - It would be possible to use these pages for microcode, although half of each 64KB page used in this way would be unused (maximum of 32KB microcode RAM inside the DSP chip).
  - NOTE!!!!!!! YOU MUST USE A ONE-TIME PROGRAM MEMORY, NOT A FLASH PROM (e.g., AT29C020) in this location (U27).
    - This is due to the function of the \PGM pin in FLASH parts and that pin's use in this application.

2.6.2 Address Latches

The DSP chip uses a multiplexed addr/data bus.

- The Addr Latches latch a 16-bit address off an 8-bit bus by following the DSP chip timing protocol.
- First the MS addr bits are latched, then the LS addr bits are latched. The 16 address bits are presented to the PROM as a parallel input to allow the DSP chip to address up to 64KB (for DTS table access).
  - In this case the upper address bit (A15) is used.
- The Micro Code Program boot sequence accesses only 32KB of this address space.
  - In this case the upper address bit (A15) is unused.
- The DSP board CPU uses this to dynamically assign usage of A15 to either a 32KB page size or a 64KB page size for optimum utilization of the PROM memory.

2.6.3 Memory Data Output Buffer

This serves to enable the data onto the multiplexed Addr/Data bus only when the DSP drives both the EXTMEM and EMOE signals.

- A 5V / 3.3V buffer chip is used to interface the 5V PROM to the 3.3V DSP chip.
- 5V PROMs are much cheaper than 3.3V PROMs so this tradeoff was made in favor of cost over I.C. count.

2.7 Analog I/O

This function provides the analog buffering between the System Analog circuits and the DACs and ADCs of the CODEC. This function consists of Input and Output buffers.

2.7.1 Input Buffers

These buffers isolate the CODEC inputs from the analog signal sources.

- The inputs are A.C. coupled to allow signals centered around 0 V to be input.
- By adding the input isolation cap, it was possible to eliminate two DC decoupling Caps on the differential outputs going into the CODEC differential inputs.
  - This is made possible by using the CODEC provided reference voltage, (CMOUT = 2.3V).
  - Op Amp output swing is around 2.3V because the CODEC is only a 5V single ended supply voltage.
- The differential input gives more total signal swing for ADC conversion (less digital conversion noise) than a single ended Op Amp would have.
- The Op Amps have a low pass filter response going into the ADC to eliminate aliasing.

2.7.2 Output Buffers

These buffers isolate the CODEC DAC outputs from the analog circuit and provide a high pass filtering function to attenuate DAC noise.

- The outputs are A.C. coupled to eliminate DC bias.

3 Production Test / Debug

3.1 Designed for In Circuit Test

The DSP board was designed to accommodate In Circuit Test due to the functional complexity of a digital bit stream decoder. For optimal test yield, ICT must be used on this board.

Following are the board design features to facilitate ICT:

- "Keep Out" space around the periphery of the board allows for the board to be seated in a vacuum fixture.
- All Components on one side of the board make fixturing simpler.
- ICT Test Pads of 36 mil size were added to the solder side of the board for 99% of board nodes.
- Inputs are independently tied high through a 10K resistor or low through a 100 Ohm resistor where a pull-up or pull-down are necessary.
- The main oscillator output is isolated by a 33 Ohm resistor to allow overdriving for dynamic test.

3.1.1 Board Revision and ICT

- Board Revision "-01" ICT test pads are masked with the solder green resist material. It is not possible to make contact with the test pads.
- Board Revision "-02" ICT test pads are unmasked, available for ICT.

3.2 "Manual" Test

There is no automated test fixture for the DSP board. The most reasonable way to test it is to install it into a known good test bed, such as Citation 5.0, Signature 2.0, or Festival 100 system and exercise the inputs and major functions. A suggested test procedure for this follows.

3.2.1 Test Strategy

- Assume that if the most complex major functions are working to exercise all inputs and outputs that the board is good.
  - Test only electrical paths and components, not design function.

3.2.2 Test Equipment

- Known good test System (Citation 5.0, Signature 2.0, or Festival 100) with one of the following monitor test setups:
  - 5.1 amplifier outputs (6 channel – Left, Right, Center, Left Surround, Right Surround, Sub-woofer) to speakers. This setup will result in the fastest test execution.
  - Alternatively, a 'scope may be used to monitor each of the System outputs (Left, Right, Center, Left Surround, Right Surround, Mono Sub-woofer) during the test. This will take more time since a

user will have to probe six outputs instead of listening to outputs simultaneously.

- AC-3 capable DVD player with:
  - AC-3 digital “coaxial” output phono jack
  - AC-3 digital TOSLINK optical output
  - Audio Output (L/R) phono jacks.
- Dolby Digital Demo and Test Disk

3.2.3 Test Setup

- Use a good quality audio cable with phono jacks to connect the DVD “coaxial” digital output phono jack to one of four DSP board SPDIF phono jacks.
- Use a TOSLINK optical cable to connect the DVD “optical” digital output to one of two DSP board TOSLINK jacks.
- Use an audio cable “pair” to link the DVD player Audio Output (L/R) phono jacks to a system audio L/R input.
  - Note: For Citation, no audio input is connected to the DSP board. If the DSP board under test is to be used ONLY in Citation 5.0, tests using this connection may be skipped.

3.2.4 Test Signal Source

- Dolby Digital Demo and Test Disk
  - Track 29, 400 Hz –20 dBFS sine wave Dolby + Pro Logic signal.
  - Track 73, 30 Hz –3 dBFS sine wave Dolby signal

3.2.5 Test Procedure

Dolby Digital Test -- tests all I.C.s functionally except analog input circuits. Note that it is necessary to test all inputs because it is possible for one of the phono jack inputs to be “bad” and the others good if the CMOS SPDIF MUX chip has suffered ESD damage.

- Adjust system volume to “20”.
- Set system to Dolby Digital mode.
- Put DVD “coaxial” output cable into DSP board Phono Jack **1**
  - Select Digital Input #1 (or on Citation, #7).
  - Run DVD Test Track 29. A 400 Hz tone should be observed in all channels (L, R, C, LS, RS) except the subwoofer channel.
  - Run DVD Test Track 73. A 30 Hz tone should be observed in the subwoofer channel.
- Put DVD “coaxial” output cable into DSP board Phono Jack **2**
  - Select Digital Input #2 (or on Citation, #8).
  - Run DVD Test Track 29. A 400 Hz tone should be observed in all channels (L, R, C, LS, RS) except the subwoofer channel.
    - If using a ‘scope, it is only necessary to check for a tone in one channel, “L”.
- Put DVD “coaxial” output cable into DSP board Phono Jack **3**
  - Select Digital Input #3 (or on Citation, #9).

    - Run DVD Test Track 29. A 400 Hz tone should be observed in all channels (L, R, C, LS, RS) except the subwoofer channel.
        - If using a ‘scope, it is only necessary to check for a tone in one channel, “L”.
- Put DVD “coaxial” output cable into DSP board Phono Jack **4**
    - Select Digital Input #4 (or on Citation, #10).
    - Run DVD Test Track 29. A 400 Hz tone should be observed in all channels (L, R, C, LS, RS) except the subwoofer channel.
        - If using a ‘scope, it is only necessary to check for a tone in one channel, “L”.
- Put DVD “optical” TOSLINK output cable into DSP board TOSLINK Input **5**
    - Select Digital Input #5 (or on Citation, #11).
    - Run DVD Test Track 29. A 400 Hz tone should be observed in all channels (L, R, C, LS, RS) except the subwoofer channel.
        - If using a ‘scope, it is only necessary to check for a tone in one channel, “L”.
- Put DVD “optical” TOSLINK output cable into DSP board TOSLINK Input **6**
    - Select Digital Input #6 (or on Citation, #12).
    - Run DVD Test Track 29. A 400 Hz tone should be observed in all channels (L, R, C, LS, RS) except the subwoofer channel.
        - If using a ‘scope, it is only necessary to check for a tone in one channel, “L”.

Dolby Pro Logic Test – tests analog input I.C.s.

- Set system to Dolby Pro Logic mode.
- Unplug all cables from DSP board digital inputs 1-6.
- Put DVD dual audio output cable into System Analog Input 1.
    - Select Analog Input #1.
    - Run DVD Test Track 29. A 400 Hz tone should be observed in all channels (L, R, C, LS, RS) except the subwoofer channel.

3.3 Debug of a board with one non-working digital input

If all but one of the inputs don’t work, it is most likely one of the following:

- If one of the phono jack inputs are not working, but all other inputs work, it is most likely one of the following:
    - Check the proper Ferrite EMI filters are installed on their pads correctly. They are a tight fit.
        - FL1 corresponds to digital input #1 (Citation input #7)
        - FL2 corresponds to digital input #2 (Citation input #8)
        - FL3 corresponds to digital input #3 (Citation input #9)
        - FL4 corresponds to digital input #4 (Citation input #10)
    - Check the proper termination resistors are installed.
        - R12 corresponds to digital input #1 (Citation input #7)
        - R13 corresponds to digital input #2 (Citation input #8)
        - R14 corresponds to digital input #3 (Citation input #9)
        - R15 corresponds to digital input #4 (Citation input #10)

- Check the proper isolation Caps are installed.
  - C18 corresponds to digital input #1 (Citation input #7)
  - C20 corresponds to digital input #2 (Citation input #8)
  - C22 corresponds to digital input #3 (Citation input #9)
  - C25 corresponds to digital input #4 (Citation input #10)
- It may be a bad CMOS Multiplexer (U10). Replace the part.

- If one of the TOSLINK inputs are not working, but all of the phono jack inputs are working:
  - First check R173 and R174 are installed and are 100 Ohms.
    - R173 corresponds to digital input #5 (Citation input #11).
    - R174 corresponds to digital input #6 (Citation input #12).
  - It may be a bad TOSLINK receiver (J1 or J2).
    - J1 corresponds to digital input #5 (Citation input #11).
    - J2 corresponds to digital input #6 (Citation input #12).
  - It may be a bad CMOS Multiplexer (U10). Replace the part.

3.4 Debug of a non-functional board

In prototype bring-up experience, if the problem is not a single bad input it is usual for the board to not work at all. There aren't usually a range of failure symptoms. Although the complexity of the board function makes it challenging to debug a failing board to a component level, there is a limited amount of debug that can be done. The following procedure gives steps to test a board that is not functioning.

NOTE: This procedure must be started from the beginning and followed in the sequence specified until the problem is found. The procedure for debug of each section assumes that the previous section was verified as good. The problem may not be found if a section is skipped.

3.4.1 Check Board Revision and Rework

- Board Revision "-01"
  - Board Silkscreen Number "40G-02036-01"
  - There must be a wire jumper between R85 and C27 on their side closest to the U31 socket.
- Board Revision "-02"
  - Board Silkscreen Number "40G-02036-02"
  - No rework required.

3.4.2 Check Critical Parts

Verify that:

- Pin 1 is oriented are differently for each of these four chips. Be sure they are all oriented properly.
- U14 is CS492603-CL
- U27 is AM27C020-90JC
  - It is programmed with the latest Crystal DSP microcode.
- U31 is N80C251SB16

- U32 is AM27C010-90JC
  - It is programmed with the latest DSP board CPU code.
- U18 is a Toshiba ‘VHC244.

3.4.3 Check On-board Voltages

If any of the on-board voltages are incorrect (except 3.3V; see below) it is either a bad connector P3 (unlikely) or a board fab problem. A fab problem in this area indicates a missing connection on an internal via. There are almost certainly other via problems on the board in this case. It recommended if this is the case that the board be scrapped.

- +5V at U6 Pin 1
- +3.3V at U6 Pin 3
  - If +5V is present but the 3.3V level is incorrect, replace the regulator U6.
- +15V at U2 Pin 8
- -15V at U2 Pin 4

3.4.4 Check the main oscillator, clock sources, and Reset Generation

Clock Generation:

- Check the main oscillator output at R1 closest to the Y1 oscillator. It should be 50 MHz with a 50% duty cycle. If not replace Y1.
- Check R1 is a 33 Ohm resistor.
- Check the 12 MHz clock at R3 closest to U7. It should be 12.288 MHz with a 50% duty cycle. If not, replace clock divider U7.
- Check R3 is a 33 Ohm resistor.

Reset Generation:

- Check the Reset is not “stuck” on. The signal level at U8-6 should be low, and U8-5 should be high.
  - If not, check U8-2; it should be high.
    - If not, check U20-2; it should be low.
      - If not, check R9 (10K) is installed.
    - Also, check U20-3; it should be low.
      - If not, check R10 (10K) is installed.
      - Also check there is NOT a jumper across SW1 terminals.
      - Also check there is NOT a switch installed for SW1. It may be a normally closed switch.
- Check a Reset pulse is generated upon power on.
  - Trigger on a positive going pulse at U8-6. You should see a positive pulse of width **29** msec.
    - If not, check C16 is 1 uF. Also check R136 is 100 Ohms.
    - Replace U8 if C16 and R136 are correct.

3.4.5 Check 80C251 Micro Controller signals and component values

- Check ALE (U31-33) is generating pulses.
  - If not, check R85 and C56 are jumpered together closest to the U31 socket (REV "-01" boards only).
- Check PSEN (U31-32) is generating pulses.
  - If not, Replace U31 (80C251)
- Check address lines at the PROM (U32 Pins 3-12, 23, & 25-29).
  - If they are "counting" in a binary fashion the CPU PROM is not oriented properly in the socket or is not programmed.
    - That is, L_CPUAD0 is toggling with a regular period of "n" msec; L_CPUAD1 is toggling with a period of "n/2"; L_CPUAD2 is toggling with a period of "n/4"; etc.
    - If so, replace the PROM.
  - If the low order address lines (U32 Pins 5-12) are always "high" or not moving, the address latch is not functional.
    - Check R138 is 100 Ohms.
    - If so, replace address latch U33.

3.4.6 Check DSP signals and component values

- Check that R50 (near U14) is 10K.
- Check that R38 (near U14) is 10K.
- Check that DSP U14-34 is at 3.3V.
  - If not, check that the FB7 Ferrite Bead (near U14) is installed.

- Check the 50 MHz clock is at DSP chip U14-30 and that its' duty cycle is 60% high / 40% low.
  - High time is less than 12 nsec and greater than 8 nsec. Corresponding Low time should be greater than 8 nsec and less than 12 nsec (total cycle time = 20 nsec).
  - If the clock is not present:
    - Check R148 (near U18) and R149 (near U18) are 100 Ohms.
    - Check R170 (near U18) is 1.8 (or 2.0) Ohms.
    - If so, replace U18.
  - If the clock IS present but the duty cycle is not acceptable or marginally meets the requirements:
    - Check U18 buffer is the proper Toshiba 74VHC244 part.
      - If U18 is not this EXACT part, replace it. There can be NO part substitutions for U18.

- Check DSP auto boot success by looking at the "EMOE_LV" signal at DSP U14-5.
  - If auto boot was initiated and successfully completed there should be no activity on this line; it should be "high".
    - If "EMOE_LV" is generating pulses continuously, the DSP code PROM U27 is not being accessed as the DSP is trying to auto boot.
      - Check DSP chip PROM U27 is oriented properly in the socket and is programmed with DSP code.
      - Check "EXTMEM_LV" U14-21 is asserted "low".
        - If not, replace the U14 DSP chip.

- Check “EMOE” at U25-11 and U26-11 has the same pulse rate as “EMOE_LV”.
  - If not, check R158 (near U35) is 100 Ohms.
  - If so, replace voltage buffer U35.
- Check R159 (near U25) and R160 (near U26) are 100 Ohms.
- Check DSP PROM low order address lines (U27 Pins 5-) ARE counting in a binary fashion.
  - That is, A0 is toggling with a regular period of “n” msec; A1 is toggling with a period of “n/2”; A2 is toggling with a period of “n/4”; etc.
  - If not, replace U25.
- Check DSP PROM upper address lines (U27 Pins 4, 23, & 25-29) ARE counting in a binary fashion.
  - If not, replace U26.
- Check PROM buffer output enable “DSPOE” at U28-1 is generating pulses.
  - If not, check R125 is 10K.
  - If so, replace U29.

- If auto boot was NOT initiated there would also be no activity on this line; it would be “high”.
  - With a ‘scope set to trigger on a negative-going pulse, power on the board. It should trigger with a series of pulses.
    - If not, replace DSP chip U14.

3.4.7 Check CODEC signals and component values

- Check that R46 & R47 (near U15) are 4.7K
- Check that R49 (near U15) is 43K
- Check that C54 (near U15) is 0.015 uF
- Check that C55 (near U15) is 1500 pF
- Check that CODEC U15-40 is at 5V.
  - If not, check that the FB8 Ferrite Bead (near U15) is installed.

- Check that the 12.288 MHz clock is present at CODEC U15-28
  - If not, go back and check the “Clock generator” section.

- With a digital signal source present on Digital Input #1 phono jack (set up as described in the earlier “Manual Test” section) check signal flow between the CODEC and DSP chip:

CODEC:

- There should be a 400 mV peak to peak SPDIF signal at CODEC SPDIF input U15-42 (use ‘scope AC coupling for this measurement only).
  - If not, check input for #1 as described in the “Input Problem” section.
- There should be a IEC967 “ttl” level signal at CODEC Serial Data Out U15-36 (use ‘scope DC coupling). This will be a series of variable width pulses.
  - If not, and all previous tests and checks have been done, replace CODEC U15.
- There should be an IEC967 “ttl” level bit clock signal at CODEC Clock Out U15-31 (approx. 1.5MHz).

- If not, and all previous tests and checks have been done, replace CODEC U15.

DSP:

- There should be an IEC967 “3.3V” level signal at DSP Serial Data In U14-22.
  - If not, check R149 (near U18) to be 100 Ohms.
  - Also if the I2S signal from U15-36 is present at U18-13 and not present at U18-7, replace buffer U18.
- There should be an IEC967 “3.3V” level bit clock signal at DSP Clock In U14-44 (approx. 1.5MHz).
  - If not, check that R51 (near U18) is 33 Ohms.
  - Also if the I2S clock signal from U15-31 is present at U18-11 and not present at U18-9, replace buffer U18.
- There should be an I2S “3.3V” level bit clock signal at DSP S Clock Out U14-43 (approx. 384KHz/sec) and LR Clock Out U14-42 (approx. 44 kHz).
  - If not, and all previous tests and checks have been done, replace DSP U14.
- There should be an I2S “3.3V” level bit data output signal at DSP Audio Data Out U14 Pins 39, 40, 41. This assumes a Dolby Digital source. This will be a series of variable width pulses.
  - If not, and all previous tests and checks have been done, replace DSP U14.

CODEC:

- There should be an I2S “ttl” level bit data input signal at CODEC Audio Data In U15 Pins 32, 33, 34. This assumes a Dolby Digital source. This will be a series of variable width pulses.
  - If not, check that DSP output MUX U16-1 is “low”
    - If not, and all previous tests and checks have been done, replace the Micro Controller expansion port chip U36.
- There should be analog outputs on CODEC Analog Outputs 1-6, U15 Pins 21-26.
  - If not, and all previous tests and checks have been done, replace CODEC U15.

3.4.8 Check Analog Buffer signals and component values

- The analog signals at the output of the CODEC should be followed through the analog buffers.
  - If there are any problems, check the appropriate Op Amps and component values.